1-MHz, Micro-Power, Low-Noise, RRIO,1.8-V CMOS OPERATIONAL AMPLIFIER Value Line Series

Check for Samples: OPA313, OPA2313, OPA4313

FEATURES

- **Low I_Q: 50 µA/ch**
- **Wide Supply Range: 1.8 V to 5.5 V**
- **Low Noise: 25 nV/√Hz at 1kHz**
- **Gain Bandwidth: 1 MHz**
- **Low Input Bias Current: 0.2 pA**
- **Low Offset Voltage: 0.5 mV**
- **Unity-Gain Stable**
- **Internal RF/EMI Filter**
- **Extended Temperature Range: –40°C to +125°C**

APPLICATIONS

- **Battery-Powered Instruments:**
  - **Consumer, Industrial, Medical**
  - **Notebooks, Portable Media Players**
- **Sensor Signal Conditioning:**
  - **Loop-Powered**
  - **Notebooks, Portable Media Players**
- **Wireless Sensors:**
  - **Home Security**
  - **Remote Sensing**
  - **Wireless Metering**

DESCRIPTION

The OPA313 family of single-, dual-, and quad-channel op amps represents a new generation of low-cost, general purpose, micro-power operational amplifiers. Featuring rail-to-rail input and output swings, and low quiescent current (50 µA, typ) combined with a wide bandwidth of 1 MHz and very low noise (25 nV/√Hz at 1 kHz) makes this family very attractive for a variety of battery-powered applications that require a good balance between cost and performance. The low input bias current supports those op amps to be used in applications with megaohm source impedances.

The robust design of the OPA313 devices provides ease-of-use to the circuit designer: unity-gain stability with capacitive loads of up to 150 pF, integrated RF/EMI rejection filter, no phase reversal in overdrive conditions, and high electrostatic discharge (ESD) protection (4kV HBM).

These devices are optimized for operation at voltages as low as +1.8 V (±0.9 V) and up to +5.5 V (±2.75 V), and are fully specified at 1.8 V, 3.3 V, and 5 V over the full extended temperature range of –40°C to +125°C.

The OPA313 (single) is available in both SC70-5 and SOT23-5 packages. The OPA2313 (dual) is offered in SO-8, MSOP-8, and DFN-8 packages. The quad-channel OPA4313 is offered in a TSSOP-14 package.

PRODUCT PREVIEW

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING
OPA313	SC70-5	DCK	–40°C to +125°C	TBD
	SOT23-5	DBV	–40°C to +125°C	TBD
OPA2313	SO-8	D	–40°C to +125°C	TBD
	MSOP-8	DGK	–40°C to +125°C	TBD
	DFN-8	DRG	–40°C to +125°C	TBD
OPA4313	TSSOP-14	PW	–40°C to +125°C	TBD

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		OPA313, OPA2313, OPA4313	UNIT
Supply voltage		7	V
Signal input terminals	Voltage(2)	(V–) – 0.5 to (V+) + 0.5	V
	Current(2)	±10	mA
Output short-circuit(3)		Continuous	mA
Operating temperature, T_A		–40 to +150	°C
Storage temperature, T_{stg}		–65 to +150	°C
Junction temperature, T_J		+150	°C
ESD rating	Human body model (HBM)	4000	V
	Charged device model (CDM)	1000	V
	Machine model (MM)	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS: V_S = +1.8 V to +5.5 V[1]

At T_A = +25 °C, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA313, OPA2313, OPA4313 MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			0.5	2.5	mV
dV_{OS}/dT	vs Temperature	T_A = –40°C to +125°C		2		µV/°C
PSRR	vs power supply	T_A = –40°C to +125°C	74	90		dB
	Channel separation, dc	At dc		10		µV/V
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	No phase reversal, rail-to-rail input	(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	T_A = –40°C to +125°C, (V_S–) – 0.2 V < V_{CM} < (V_S+) – 1.3 V	70	85		dB
		V_S = 1.8 V, V_{CM} = -0.2V to +1.8V	58	73		dB
		T_A = –40°C to +125°C, V_S = 1.8 V, V_{CM} = -0.2V to +1.6V	58	70		dB
		T_A = –40°C to +125°C, V_S = 5.5 V, V_{CM} = –0.2 V to 5.7 V[2]	64	80		dB
INPUT BIAS CURRENT						
I_B	Input bias current			±0.2	±10	pA
		T_A = –40°C to +85°C			±50	pA
		T_A = –40°C to +125°C			±600	pA
I_{OS}	Input offset current			±0.2	±10	pA
		T_A = –40°C to +85°C			±50	pA
		T_A = –40°C to +125°C			±600	pA
NOISE						
	Input voltage noise (peak-to-peak)	f = 0.1 Hz to 10 Hz		6		μV_{PP}
e_n	Input voltage noise density	f = 10 kHz		22		$nV/\sqrt{Hz}$
		f = 1 kHz		25		$nV/\sqrt{Hz}$
i_n	Input current noise density	f = 1 kHz		5		$fA/\sqrt{Hz}$
INPUT CAPACITANCE						
C_{IN}	Differential			1		pF
	Common-mode			5		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	T_A = –40°C to +125°C, V_S = 1.8 V, 0.1 V < V_O < (V+) – 0.1 V	90	110		dB
		T_A = –40°C to +125°C, V_S = 5.5 V, 0.1 V < V_O < (V+) – 0.1 V	104	116		dB
		T_A = –40°C to +125°C, V_S = 1.8 V, 0.3 V < V_O < (V+) – 0.3 V, R_L = 2 kΩ[2]	90	100		dB
		T_A = –40°C to +125°C, V_S = 5.5 V, 0.3 V < V_O < (V+) – 0.3 V, R_L = 2 kΩ[2]	100	110		dB
	Phase margin	V_S = 5.0 V, G = +1		65		degrees

(1) Parameters with minimum or maximum specification limits are 100% production tested at +25ºC, unless otherwise noted. Over temperature limits are based on characterization and statistical analysis.
(2) Specified by design and characterization; not production tested.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS: V_S = +1.8 V to +5.5 V[1] (continued)

At T_A = +25 °C, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA313, OPA2313, OPA4313			UNIT
			MIN	TYP	MAX	
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	V_S = 1.8 V, C_L = 10 pF		0.9		MHz
		V_S = 5.0 V, C_L = 10 pF		1		MHz
SR	Slew rate	V_S = 1.8 V, G = +1		0.45		V/µs
		V_S = 5.0 V, G = +1		0.5		V/µs
t_S	Settling time	To 0.1%, V_S = 5.0 V, 2-V step , G = +1		5		µs
		To 0.01%, V_S = 5.0 V, 2-V step , G = +1		6		µs
	Overload recovery time	V_S = 5.0 V, V_{IN} × Gain > V_S		3		µs
THD+N	Total harmonic distortion + noise[3]	V_S = 5.0 V, V_O = 1 V_{RMS}, G = +1, f = 1 kHz		TBD %		
OUTPUT						
V_O	Voltage output swing from supply rails	V_S = 1.8 V, R_L = 100 kΩ[4]		5	15	mV
		V_S = 5.5 V, R_L = 100 kΩ[4]		5	20	mV
		T_A = –40°C to +125°C, R_L = 100 kΩ[4]			30	mV
		V_S = 1.8 V, R_L = 2 kΩ[4]		25	50	mV
		V_S = 5.5 V, R_L = 2 kΩ[4]		75	100	mV
		T_A = –40°C to +125°C, R_L = 2 kΩ			125	mV
I_{SC}	Short-circuit current	V_S = 1.8 V		±6		mA
		V_S = 5.5 V		±15		mA
		T_A = –40°C to +125°C, V_S = 5.5 V		±12		mA
R_O	Open-loop output impedance			2300		Ω
POWER SUPPLY						
V_S	Specified voltage range		1.8 (±0.9)		5.5 (±2.75)	V
I_Q	Quiescent current per amplifier	I_O = 0 mA		50	60	µA
		T_A = –40°C to +125°C, V_S = 5.0 V, I_O = 0 mA			85	µA
	Power-on time	V_S = 0 V to 5 V, to 90% I_Q level		TBD		µs
TEMPERATURE						
	Specified range		–40		+125	°C
	Operating range		–40		+150	°C
	Storage range		–65		+150	°C

(3) Third-order filter; bandwidth = 80 kHz at –3 dB.
(4) Specified by design and characterization; not production tested.

PRODUCT PREVIEW

THERMAL INFORMATION: OPA313

THERMAL METRIC(1)		OPA313		UNITS
		DBV (SOT23)	DCK (SC70)	
		5 PINS	5 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	228.5	281.4	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	99.1	91.6	
θ_{JB}	Junction-to-board thermal resistance	54.6	59.6	
ψ_{JT}	Junction-to-top characterization parameter	7.7	1.5	
ψ_{JB}	Junction-to-board characterization parameter	53.8	58.8	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

THERMAL INFORMATION: OPA2313

THERMAL METRIC(1)		OPA2313			UNITS
		D (SO)	DGK (MSOP)	DRB (DFN)	
		8 PINS	8 PINS	8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	138.4	191.2	53.8	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	89.5	61.9	69.2	
θ_{JB}	Junction-to-board thermal resistance	78.6	111.9	20.1	
ψ_{JT}	Junction-to-top characterization parameter	29.9	5.1	3.8	
ψ_{JB}	Junction-to-board characterization parameter	78.1	110.2	20.0	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	11.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

THERMAL INFORMATION: OPA4313

THERMAL METRIC(1)		OPA4313	UNITS
		PW (TSSOP)	
		14 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	121.0	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	49.4	
θ_{JB}	Junction-to-board thermal resistance	62.8	
ψ_{JT}	Junction-to-top characterization parameter	5.9	
ψ_{JB}	Junction-to-board characterization parameter	62.2	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	

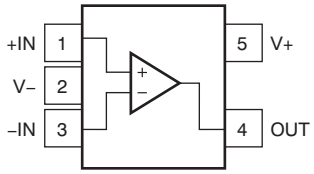
(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

PRODUCT PREVIEW

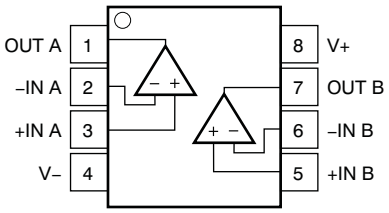
PRODUCT PREVIEW

PIN CONFIGURATIONS

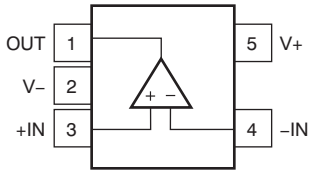
DCK PACKAGE
SC70-5
(TOP VIEW)



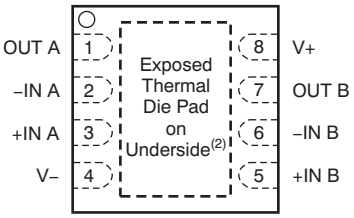
D, DGK PACKAGES
SO-8, MSOP-8
(TOP VIEW)



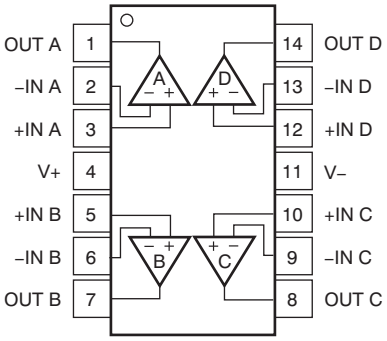
DBV PACKAGE
SOT23-5
(TOP VIEW)



DRG PACKAGE(1)
DFN-8
(TOP VIEW)



PW PACKAGE
TSSOP-14
(TOP VIEW)



(1) Pitch: 0,65 mm.

(2) Connect thermal pad to V–. Pad size: 1,8 mm × 1,5 mm.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
OPA2313ID	PREVIEW	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA2313IDGK	PREVIEW	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
OPA2313IDGKR	PREVIEW	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
OPA2313IDR	PREVIEW	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA2313IDRGR	PREVIEW	SON	DRG	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA2313IDRGT	PREVIEW	SON	DRG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

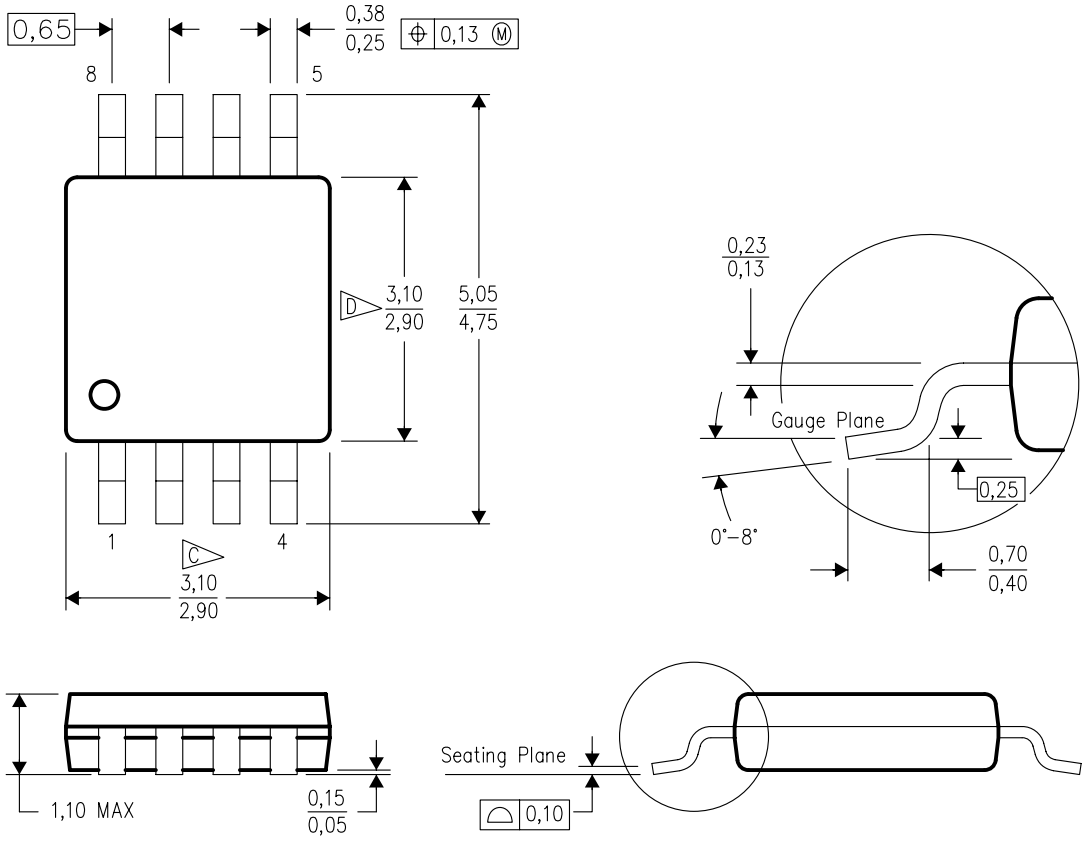
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

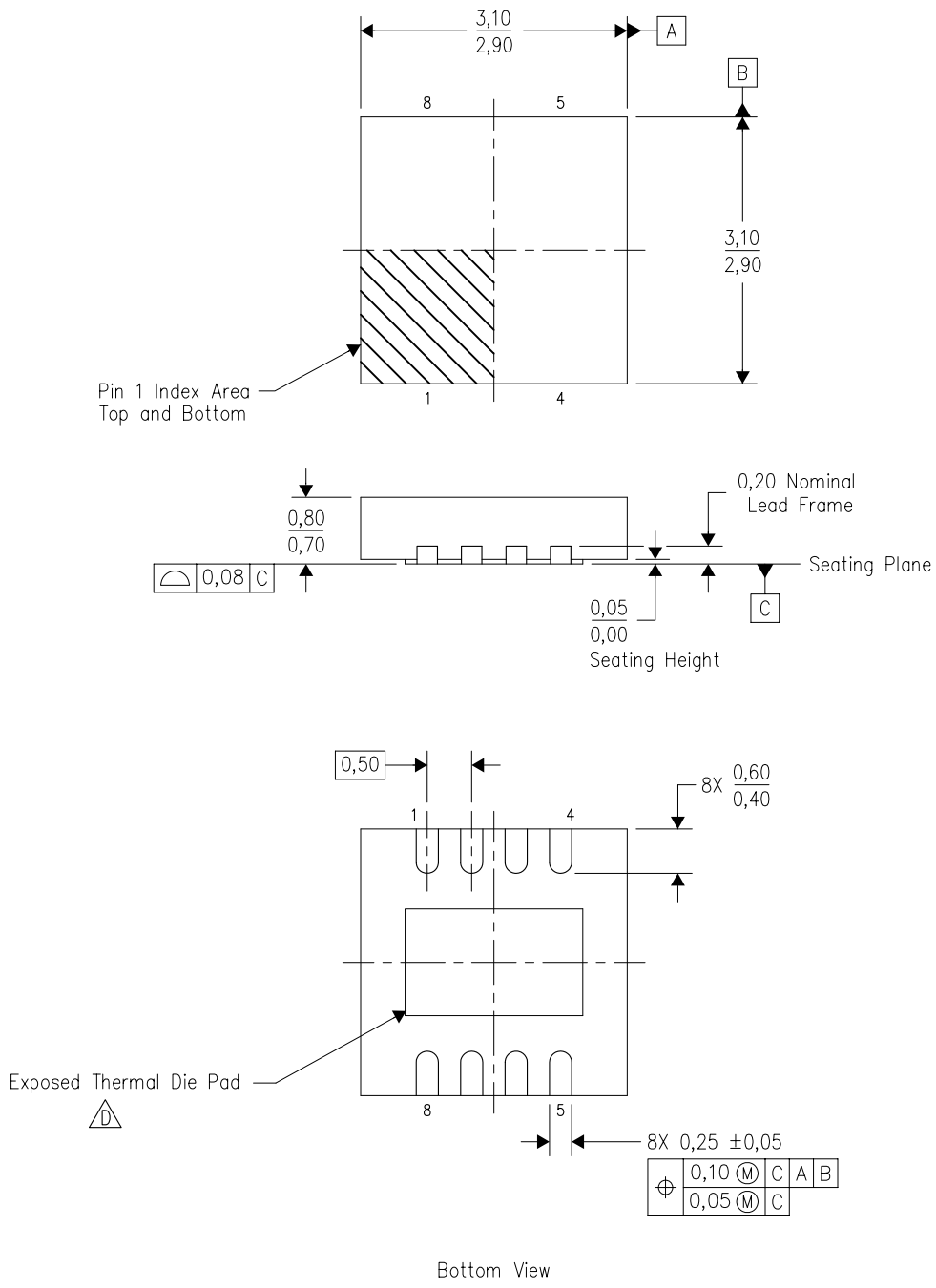
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

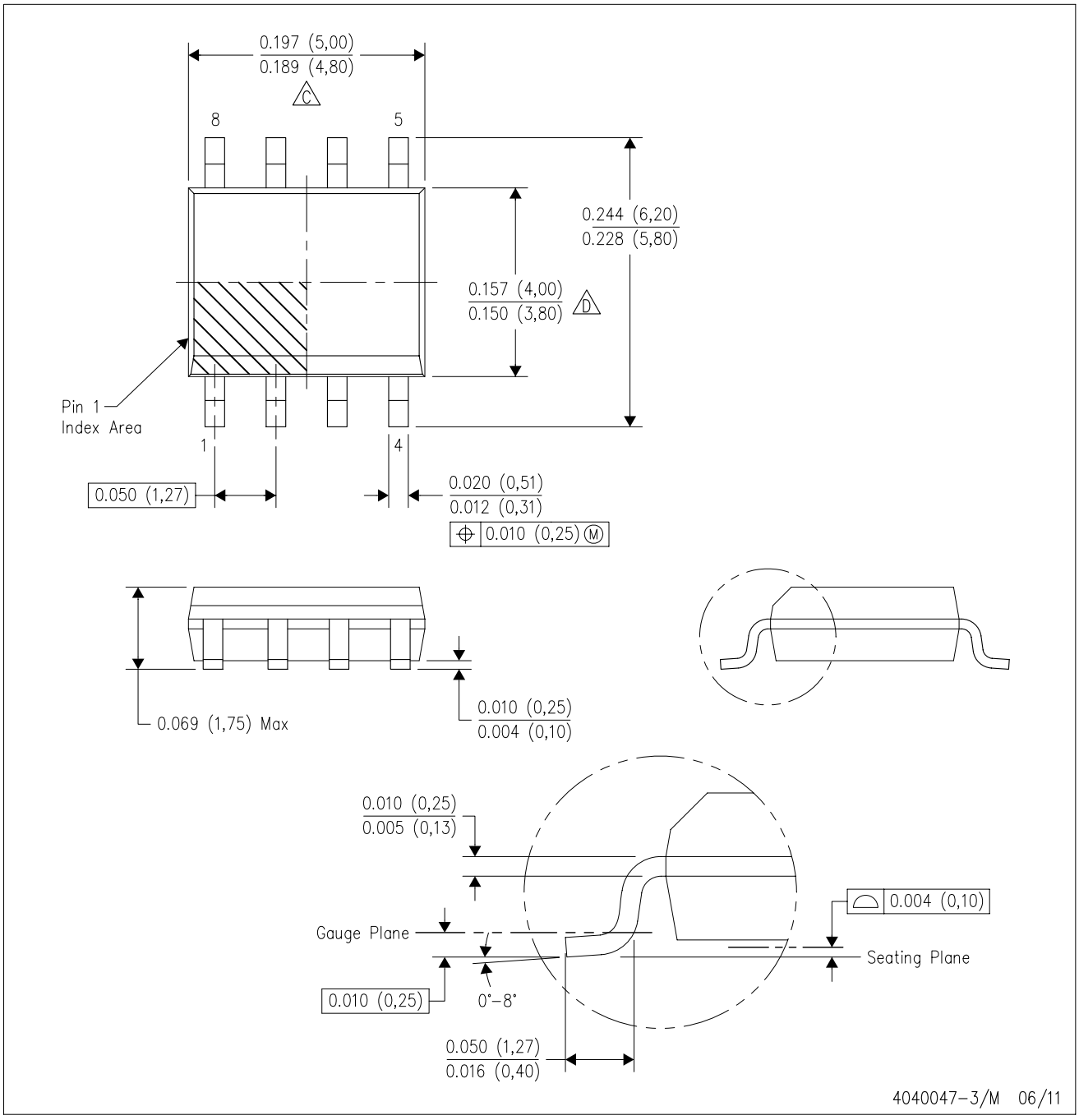
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. JEDEC MO–229 package registration pending.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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